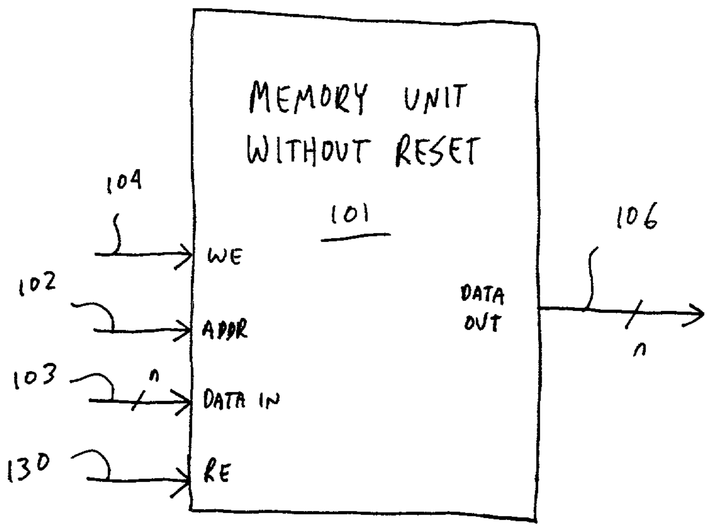
MEMORY UNIT
WITHOUT RESET
101
104
WE
102
ADDR
103
n
DATA IN
130
RE
DATA
OUT
106
n

FIGURE 1

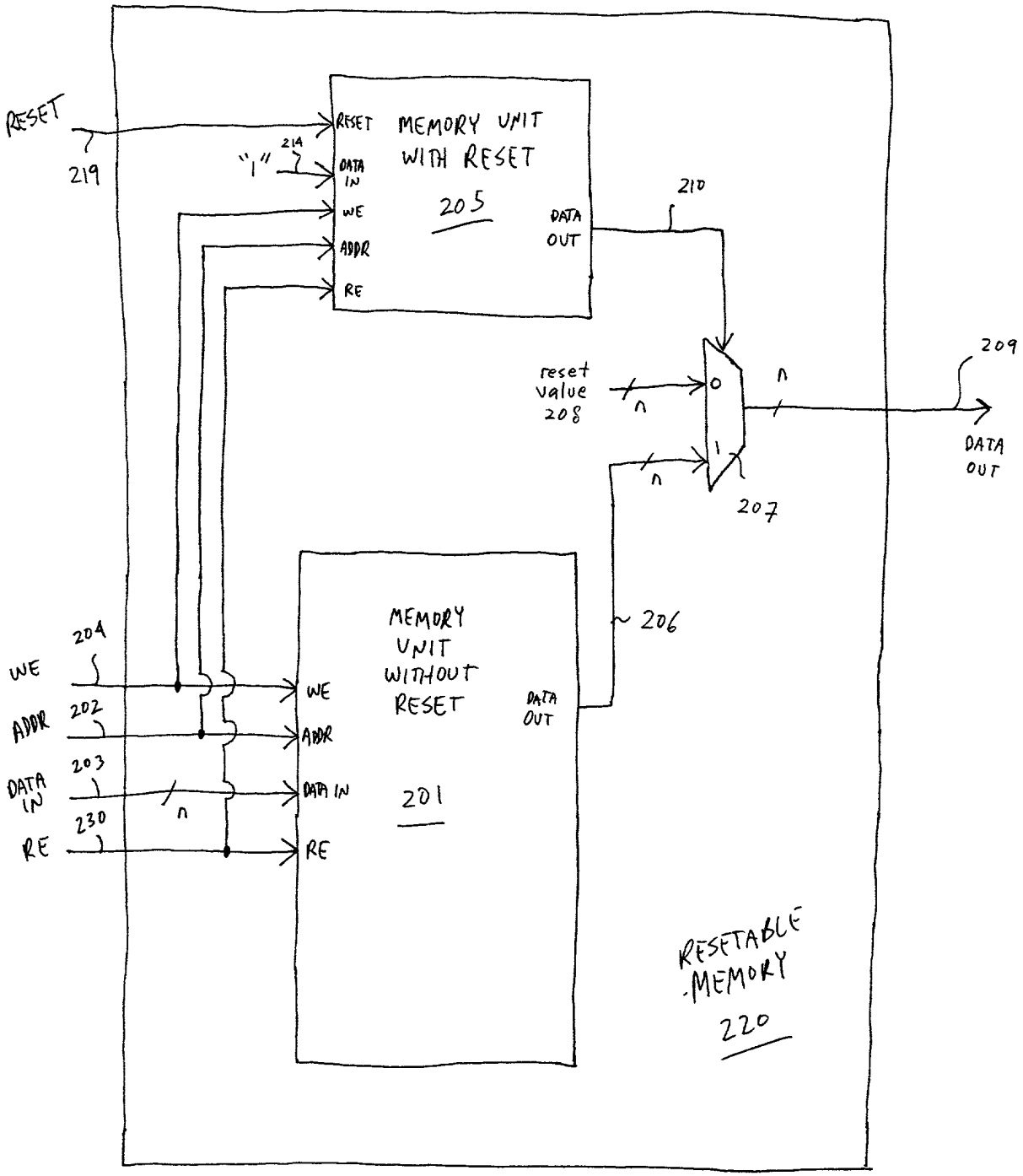

FIGURE 2A

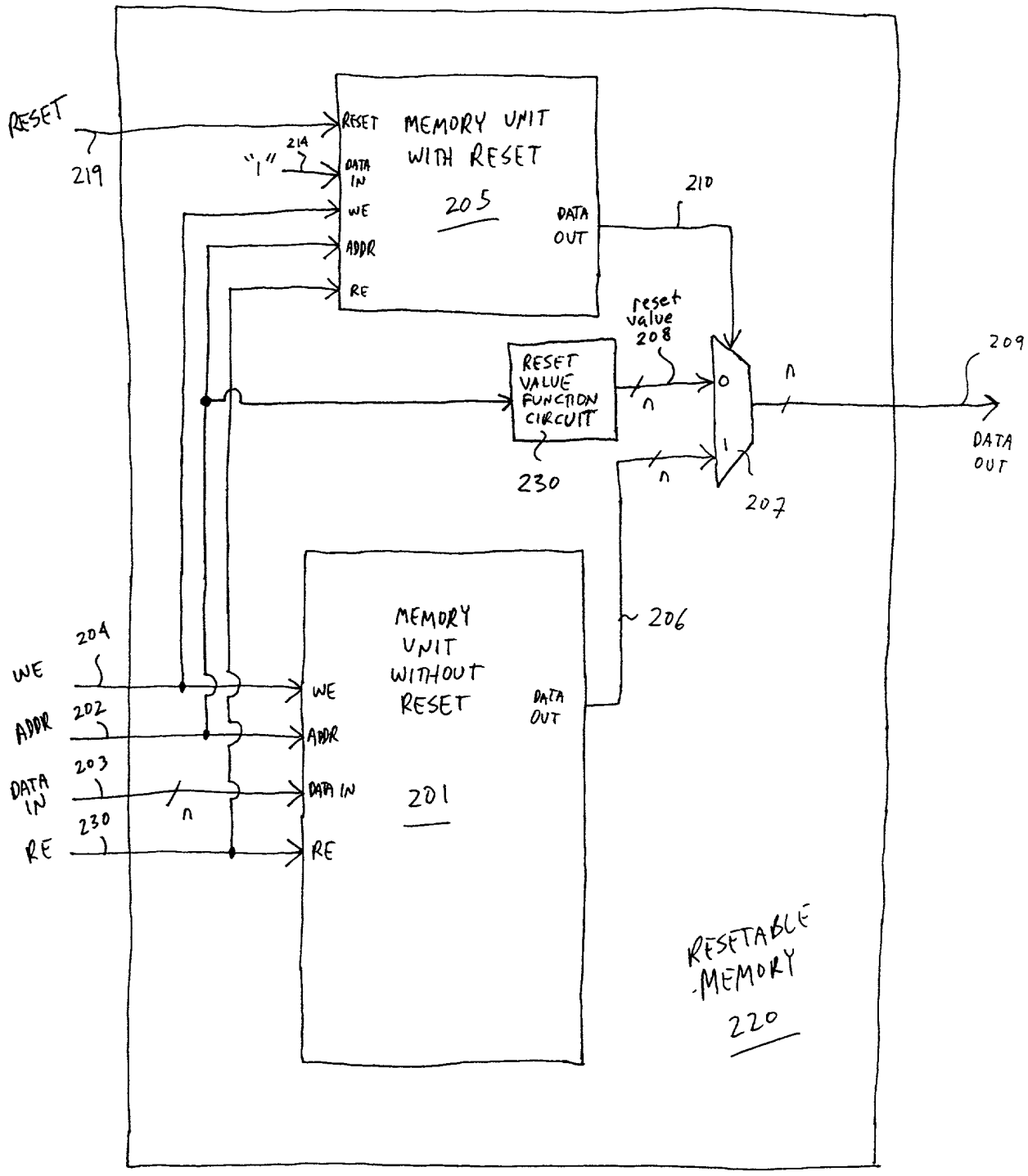
RESET
219
"1"
214
RESET
DATA IN
WE
ADDR
RE
MEMORY UNIT WITH RESET
205
DATA OUT
210
reset value 208
RESET VALUE FUNCTION CIRCUIT
230
n
0
1
207
209
DATA OUT
206
MEMORY UNIT WITHOUT RESET
201
WE
204
ADDR
202
DATA IN
203
RE
230
RESETABLE MEMORY
220

FIGURE 2B

```
module synReset(data_in, addr, reset, we, clk, data_out);

parameter data_width = 1024;
parameter addr_width = 10;
parameter RAMsize = 8;
parameter reset_value = 8'D0;

input [data_width-1:0] data_in;
input [addr_width-1:0] addr;
input reset, we, clk;
output [data_width-1:0] data_out;

integer i;
reg [data_width-1:0] mem [RAMsize-1:0];
wire [data_width-1:0] data_out;
//synthesis loop_limit 2000
always @(posedge clk)
begin
        if(reset == 1'b1)
        begin
                for (i=0; i < RAMsize ; i=i+1)
                        begin
                                mem[i] = reset_value;
                        end
        end else if(we == 1'b1)
        begin
                        mem[addr] = data_in;
        end
end
assign data_out = mem[addr];
endmodule
```

FIGURE 2C

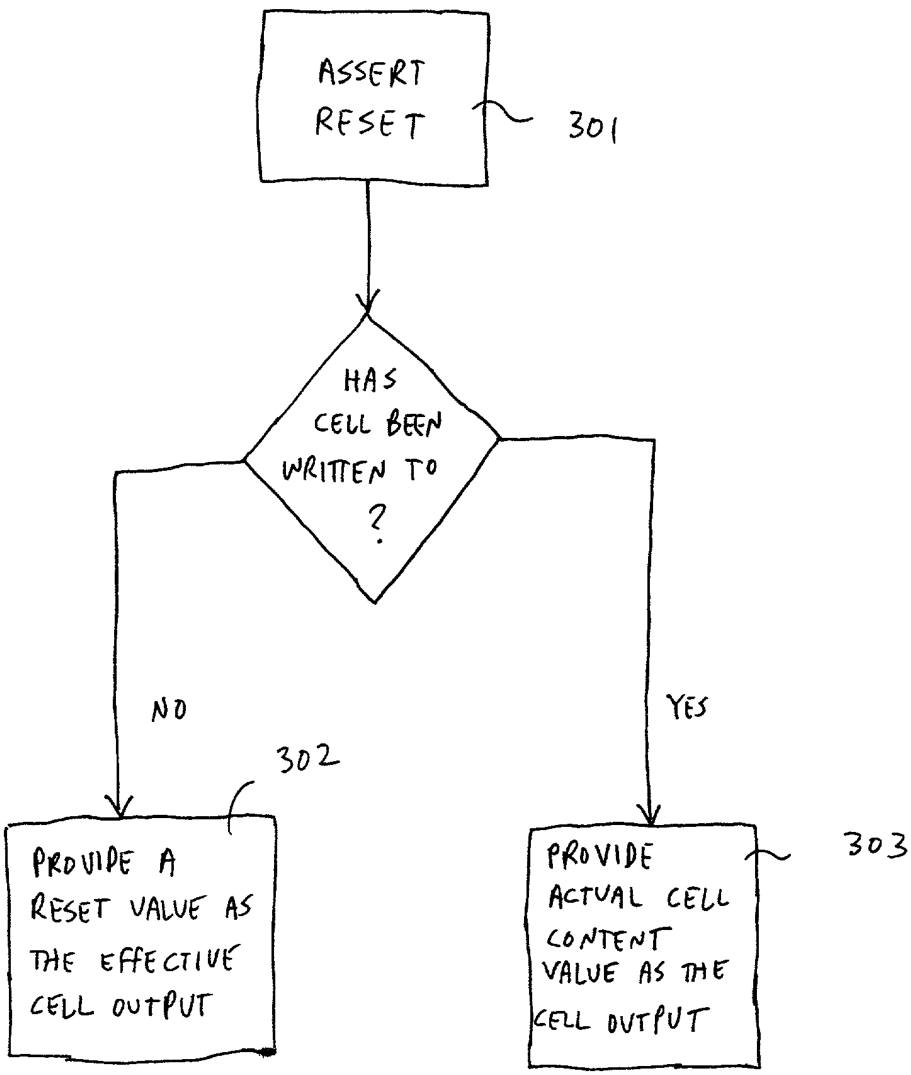
ASSERT RESET
301
HAS CELL BEEN WRITTEN TO ?
NO
YES
302
PROVIDE A RESET VALUE AS THE EFFECTIVE CELL OUTPUT
303
PROVIDE ACTUAL CELL CONTENT VALUE AS THE CELL OUTPUT

FIGURE 3

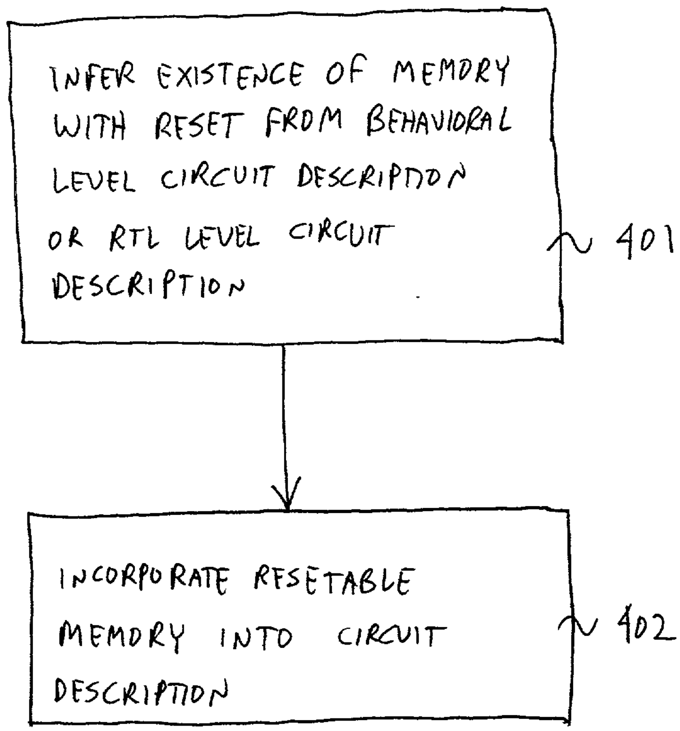
INFER EXISTENCE OF MEMORY WITH RESET FROM BEHAVIORAL LEVEL CIRCUIT DESCRIPTION OR RTL LEVEL CIRCUIT DESCRIPTION
401
INCORPORATE RESETABLE MEMORY INTO CIRCUIT DESCRIPTION
402

FIGURE 4

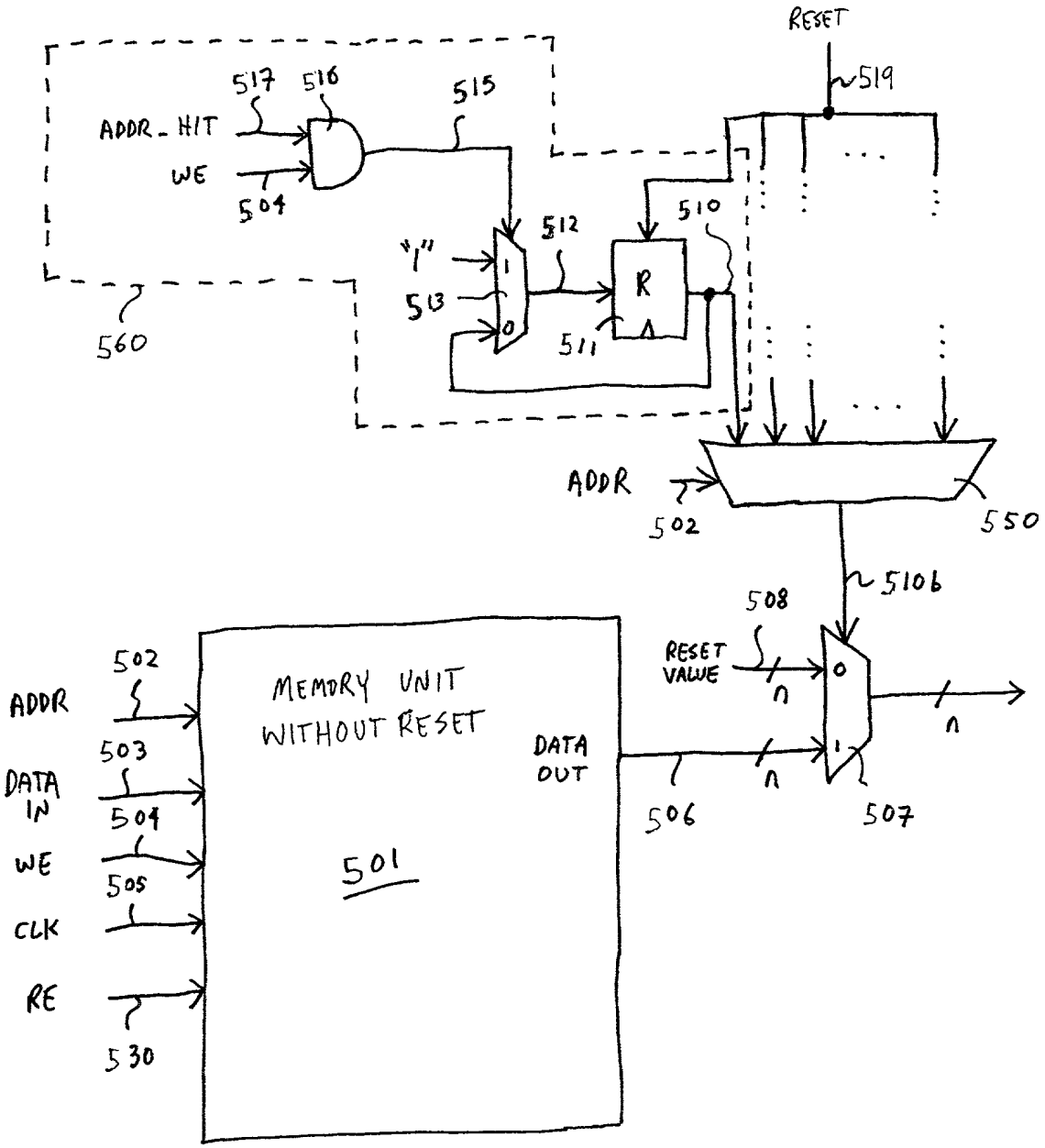

FIGURE 5

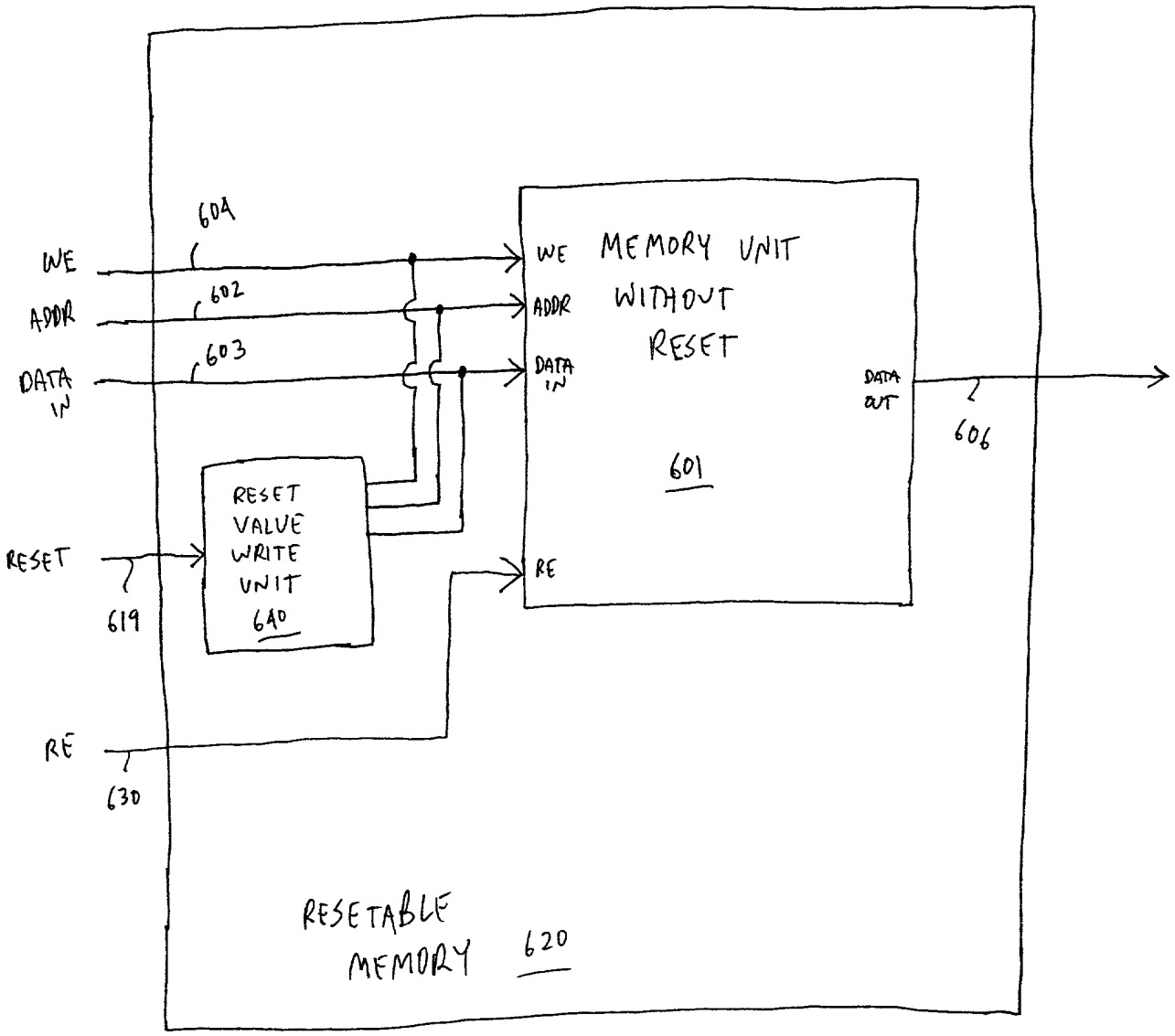

FIGURE 6

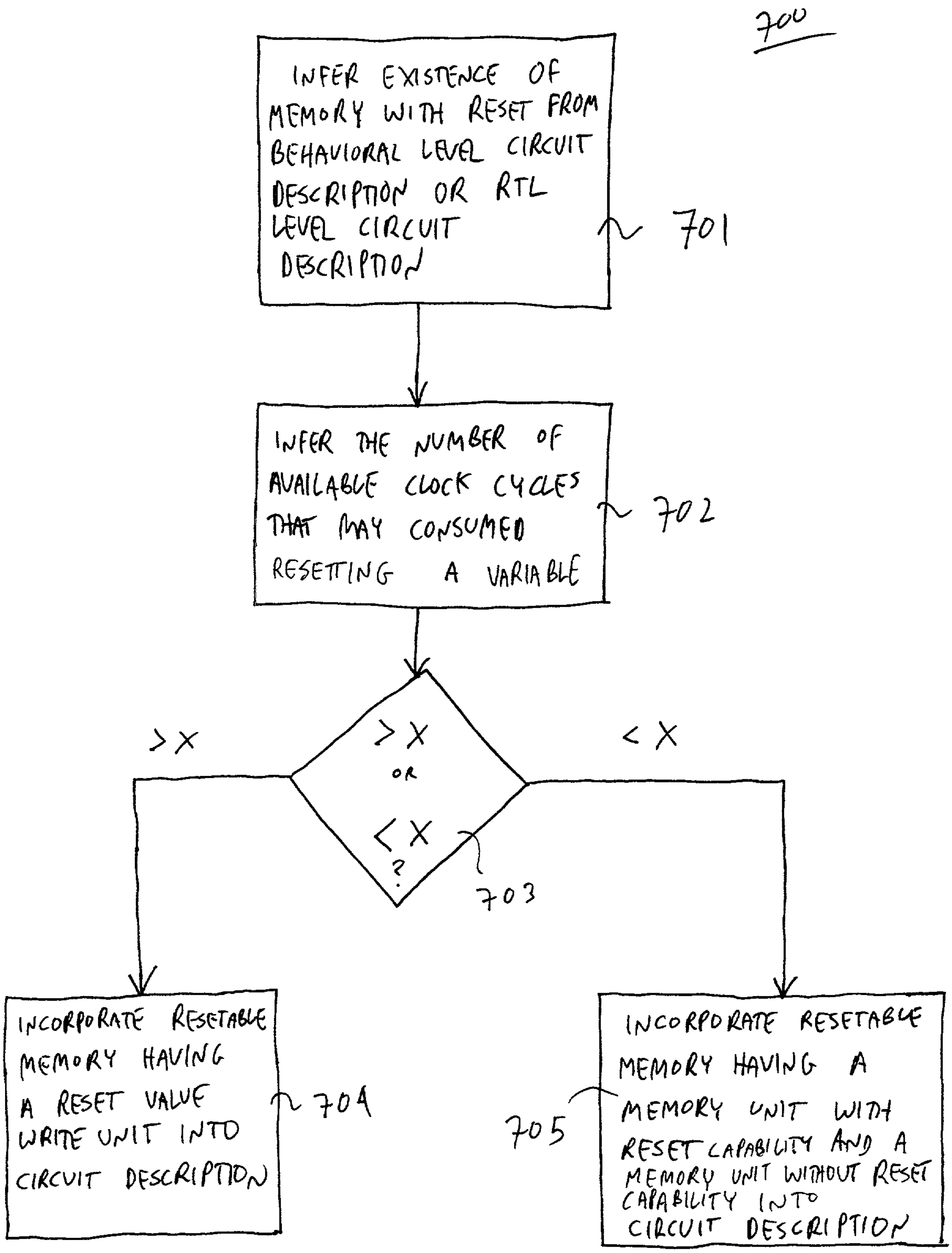
700
INFER EXISTENCE OF MEMORY WITH RESET FROM BEHAVIORAL LEVEL CIRCUIT DESCRIPTION OR RTL LEVEL CIRCUIT DESCRIPTION
701
INFER THE NUMBER OF AVAILABLE CLOCK CYCLES THAT MAY CONSUMED RESETTING A VARIABLE
702
> X OR < X ?
703
> X
< X
INCORPORATE RESETABLE MEMORY HAVING A RESET VALUE WRITE UNIT INTO CIRCUIT DESCRIPTION
704
INCORPORATE RESETABLE MEMORY HAVING A MEMORY UNIT WITH RESET CAPABILITY AND A MEMORY UNIT WITHOUT RESET CAPABILITY INTO CIRCUIT DESCRIPTION
705

FIGURE 7

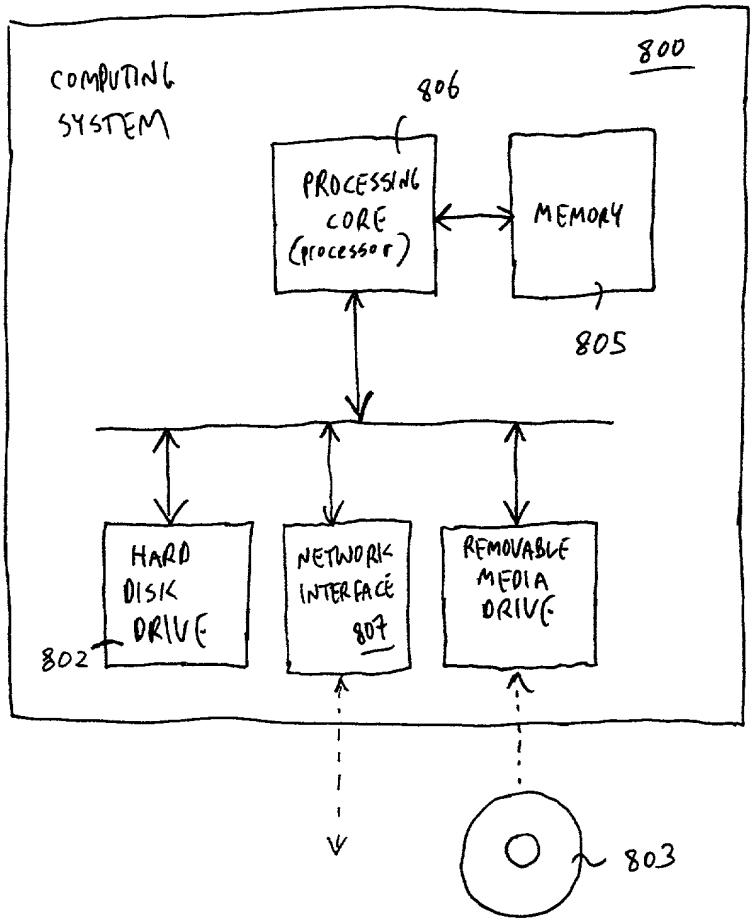
800
COMPUTING SYSTEM
806
PROCESSING CORE (processor)
MEMORY
805
HARD DISK DRIVE
802
NETWORK INTERFACE
807
REMOVABLE MEDIA DRIVE
803

FIGURE 8